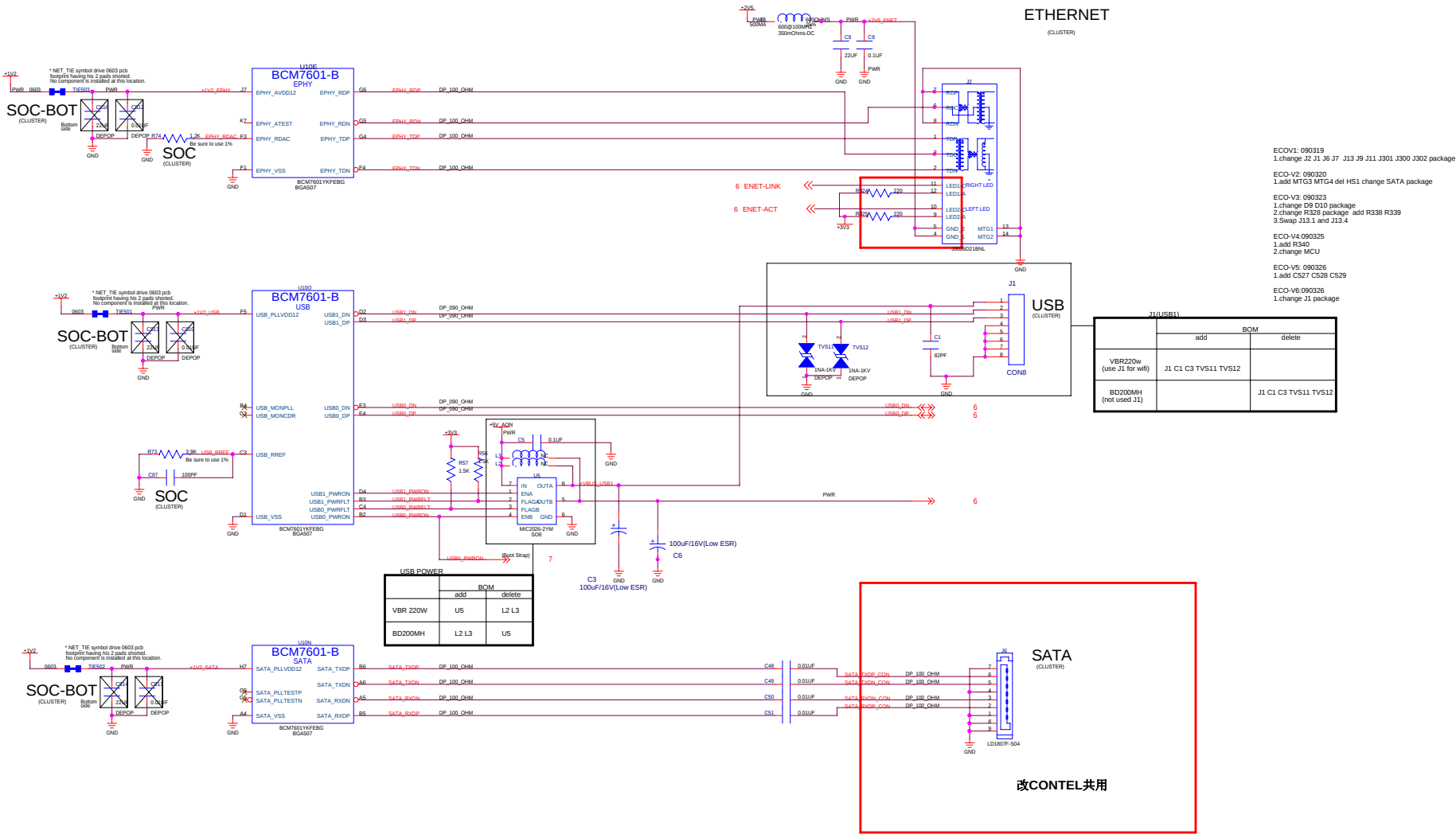
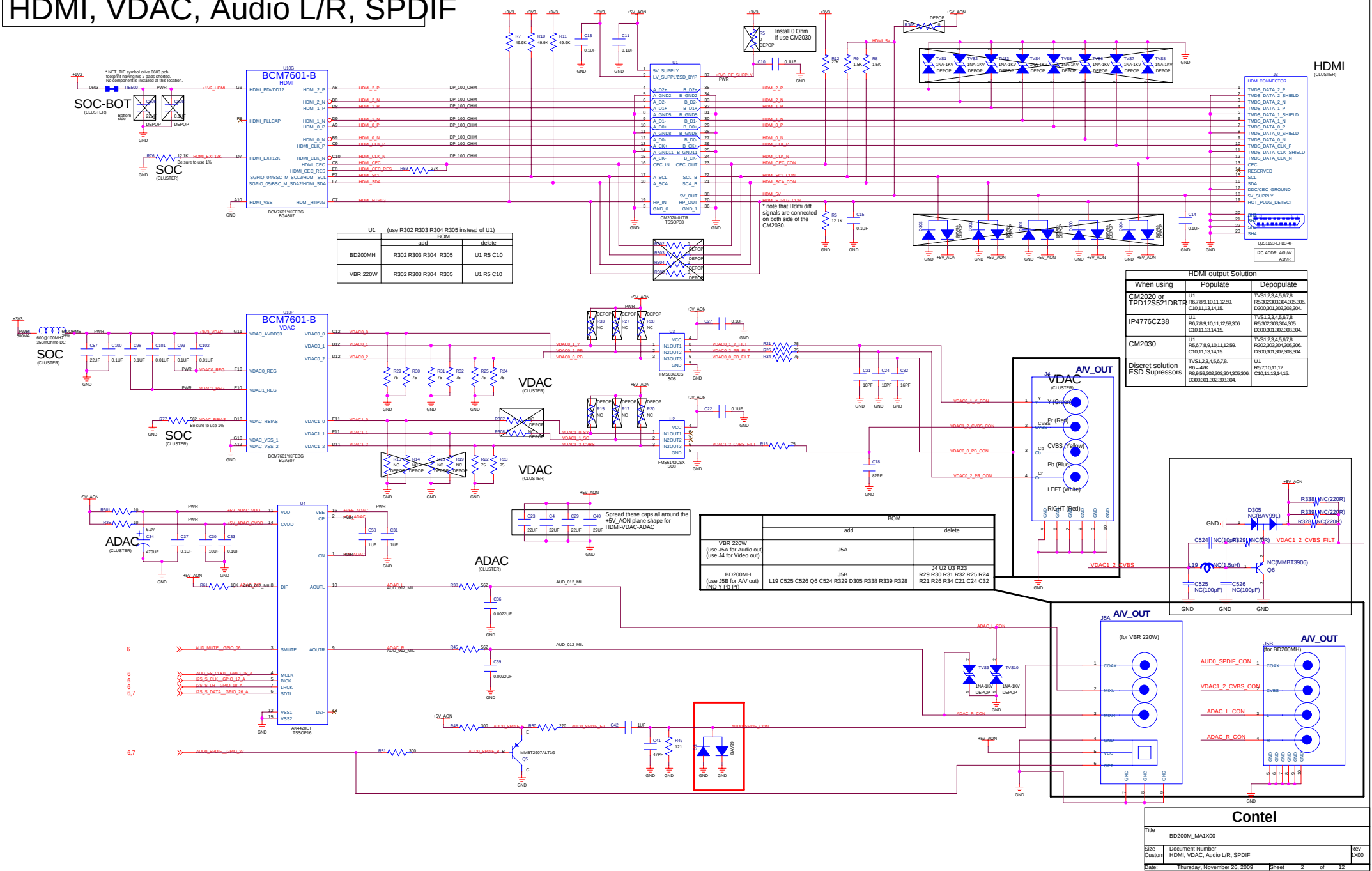


Ethernet, USB, SATA

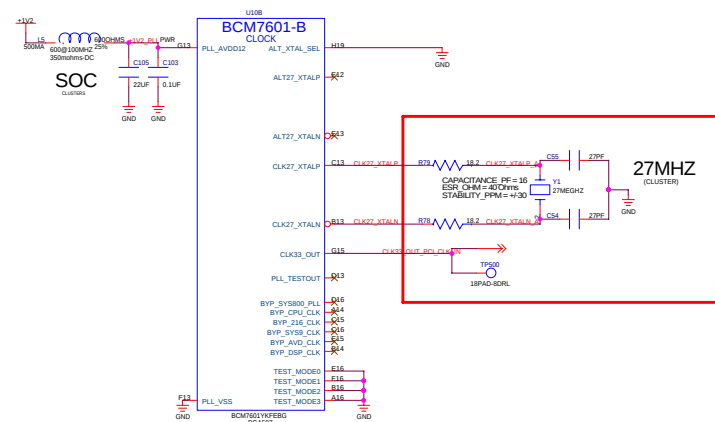


Contel		
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HDMI, VDAC, Audio L/R, SPDIF



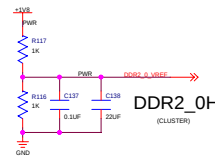
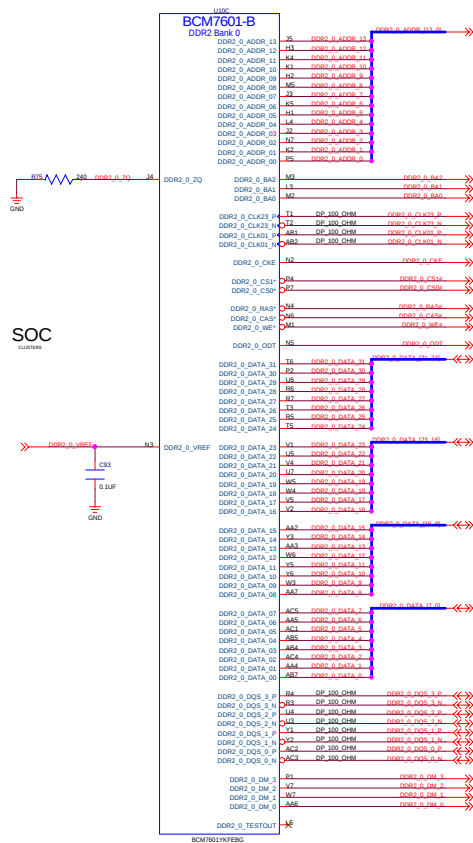
Clock



This NAND device uses only CE0.
Up to 4 CE are routed to the NAND package
to support multiple CE NAND devices.

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DDR2 Bank-0



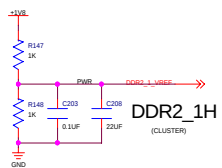
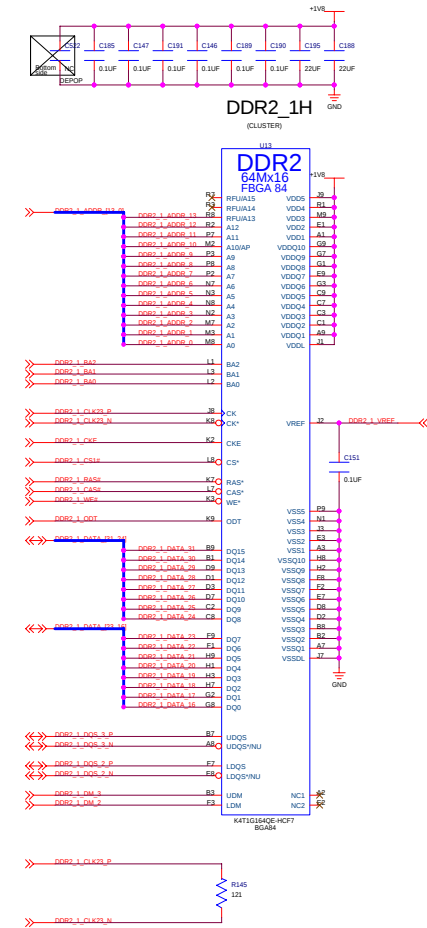
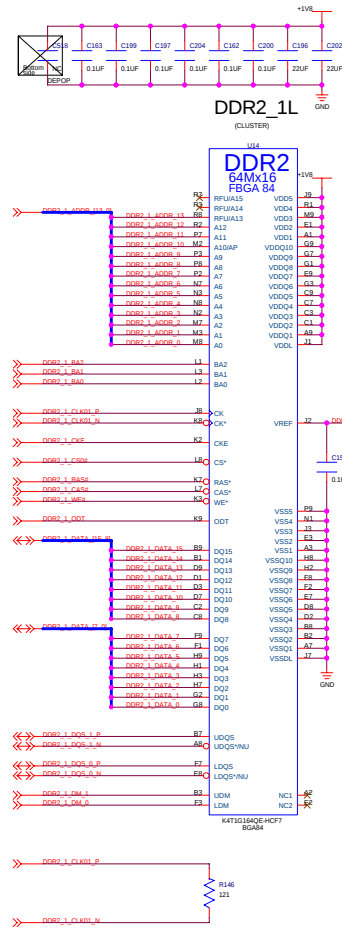
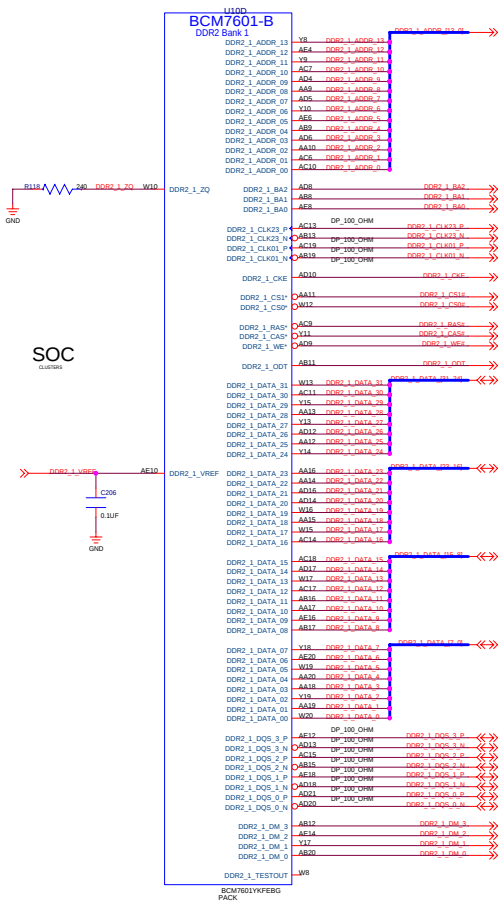
BCM7601 DDR2 2x16 --> Design notes and Layout Guidelines:

- 1- Length of all Data signals into a Byte Lane should be matched together (<300 mils).
- 2- Length of all Data signals between Byte Lane should be matched together (<550 mils).
- 3- DDR2 clock and DQS P/N traces must be routed as 100 Ohms Differential pairs. Traces width and gap according to PCB stackup.
- 4- When developing the PCB floor plan, the proximity of the DDR2 device to the memory controller is an important factor. If the memory is close to the controller, the layout is usually easier.
 - To avoid the use of external address termination on high-speed DDR2, the target address trace length should be 2.3in or less.
 - To avoid the use of external data termination on high-speed DDR2, the target data trace length should be 1.3in or less.

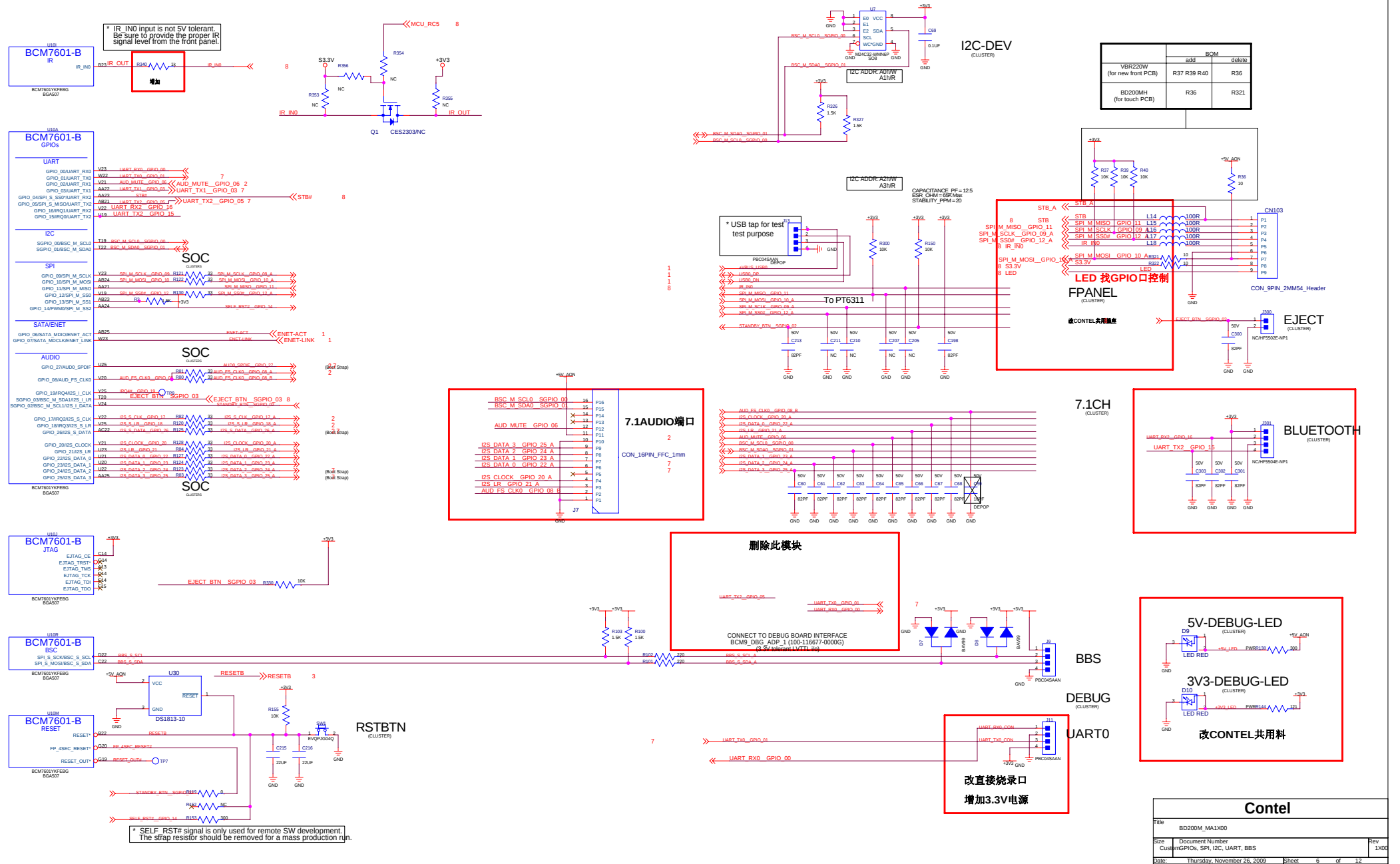
* If those requirements can not be reached, refer to JEDEC JESD79-2B standard for design rules and terminations.

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DDR2 Bank-1



7.1 Card, FPanel, GPIOs, SPI, I2C, UART, BBS, JTAG, Reset, LED, BT-Con, FEject-Con

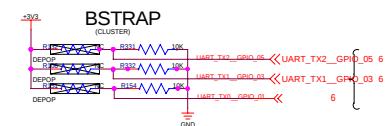
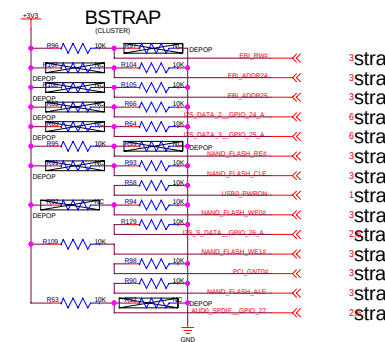


Boot Strap Options

SUN_TOP_CTRL.SUN_TOP_CTRL_STRAP		VALUE 0 = C0080481	
Field Name	Signal Name	Bit Field	Field Description
1 strap_use_defaults	EBI_RW#	31	Force usage of default values for strap signals 0 = All straps must be set on board 1 = Only non-default values need be set
1 strap_reset_outb_def_valu	Internal (Hard Coded)	30	Default value of the reset_outb pin after hardware reset After hardware reset, the reset_outb pin will change to 1 (deasserted)
0 strap_test_debug_en_1	EBI_ADDR24	29	Test debug mode select
0 strap_test_debug_en_0	EBI_ADDR25	28	Security related (2 bits) ?default = 0
0 Reserved	N/A	27	Reserved bit must be written with 0. A read returns an unknown value.
0 strap_33_27_mhz_clock	Internal (Hard Coded)	26	33 MHz clock is used
0 Reserved	N/A	25	Reserved bit must be written with 0. A read returns an unknown value.
0 strap_xtal_sel	Refer to pin ALT_XTAL_SEL	24	XTAL select
0 strap_xtal_adj_3		23	
0 strap_xtal_adj_2	I2S_DATA_2__GPIO_24_A	22	
0 strap_xtal_adj_1	I2S_DATA_3__GPIO_25_A	21	XTAL adjustment (This strap has no effect when using ALT_XTAL).
0 strap_xtal_adj_0		20	
1 strap_ebi_rom_size_1	NAND_FLASH_RE#	19	NAND ROM: 0 = NOR flash 1 = OneNAND flash 2 = reserved 3 = reserved
0 strap_ebi_rom_size_0	NAND_FLASH_CLE	18	NAND ROM: 0 = Disable ECC 1 = 1 bit ECC 2 = 4 bit ECC 3 = 8 bit ECC
0 strap_ebi_invert_addr	USB0_PWRON	17	0 = Do not invert EBI address 1 = Invert upper bits of EBI address (Not used by NAND flash)
0 Reserved	N/A	16	
0 Reserved	N/A	15	Reserved bit must be written with 0. A read returns an unknown value.
0 strap_pci_ext_arb	Internal (Hard Coded)	14	Internal Arb. (default)
0 strap_flash_width	NAND_FLASH_WE0#	13	NAND ROM: 0 = 8 bit 1 = 16 bit
0 strap_system_big_endian	I2S_S_DATA__GPIO_26_A	12	0 = Chip is operating as a little endian device in a little endian system 1 = Chip is operating as a big endian device in a big endian system
0 strap_ebi_cs_swap	Internal (Hard Coded)	11	0 = no swap 1 = swap cs_0 and cs_1
1 strap_nand_flash	NAND_FLASH_WE1#	10	0 = Boot from NAND 1 = Boot from NAND
0 strap_spi_slave_enable	PCI_GNT0#	9	0 = The SSP uses SPI protocol 1 = The SSP uses SPI protocol
0 strap_pci_memwin_size_1	Internal (Hard Coded)	8	Internal (Hard Coded)
1 strap_pci_memwin_size_0	Internal (Hard Coded)	7	1024 MB
0 strap_pci_memwin2_en	Internal (Hard Coded)	6	PCI memory window 2 is disabled
0 strap_pci_memwin1_en	Internal (Hard Coded)	5	PCI memory window 1 is enabled
0 strap_pci_client	NAND_FLASH_ALE	4	0 = Chip is a PCI master device 1 = Chip operates as a PCI slave device
0 Reserved	N/A	3	
0 Reserved	N/A	2	
0 Reserved	N/A	1	Reserved bit must be written with 0. A read returns an unknown value.
1 strap_reset_ext_mode	AUD0_SPDIF__GPIO_27	0	0 = reset_outb is not extended 1 = reset_outb is extended 300 ms

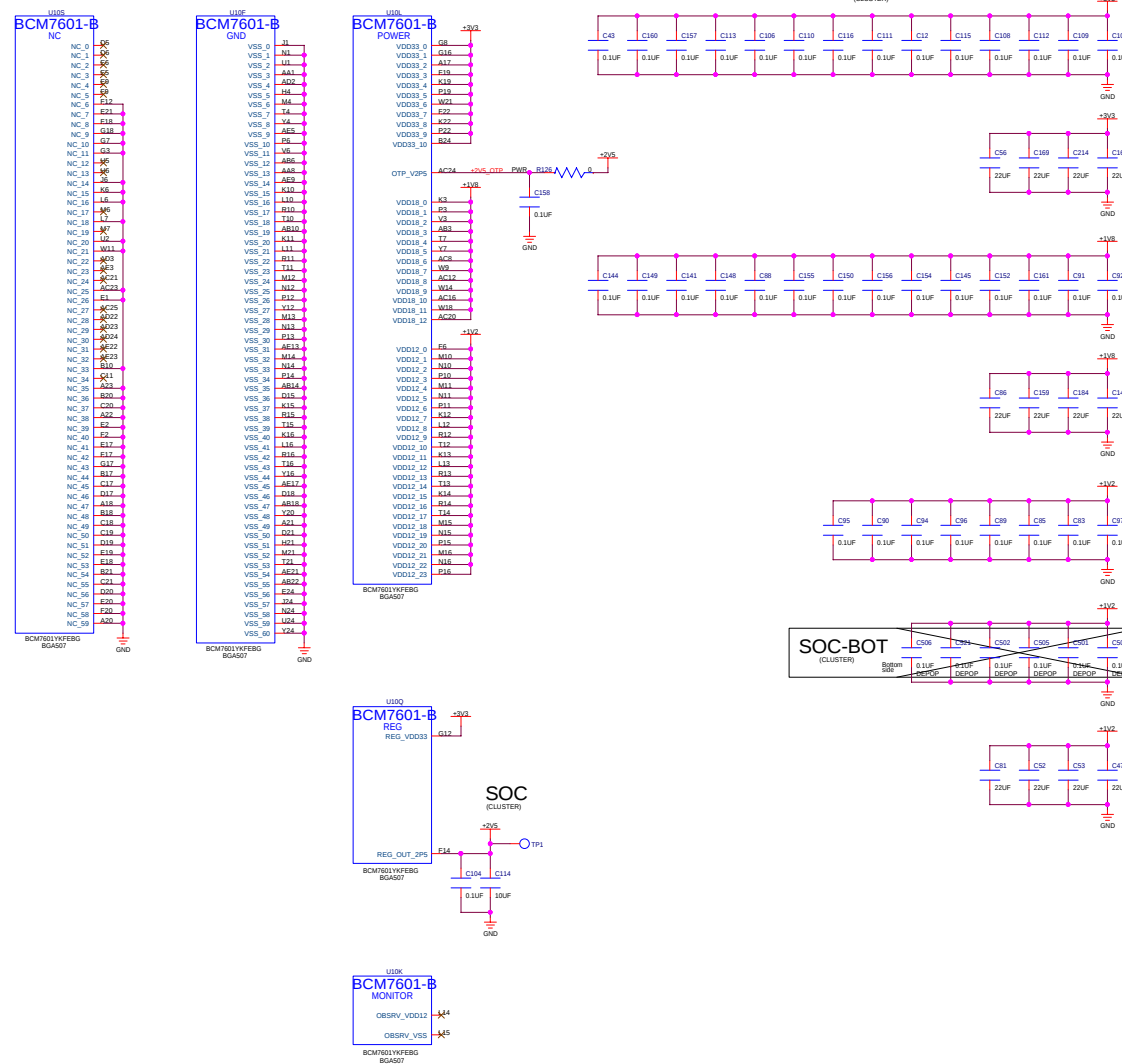
Boot strap option -> Design notes and Layout Guidelines:

- 1- Note these configuration resistors do not need to be close to the BCM7601. So, place them at the destination of the trace. It will clear the BCM7601 area and help the fanout of the chip.

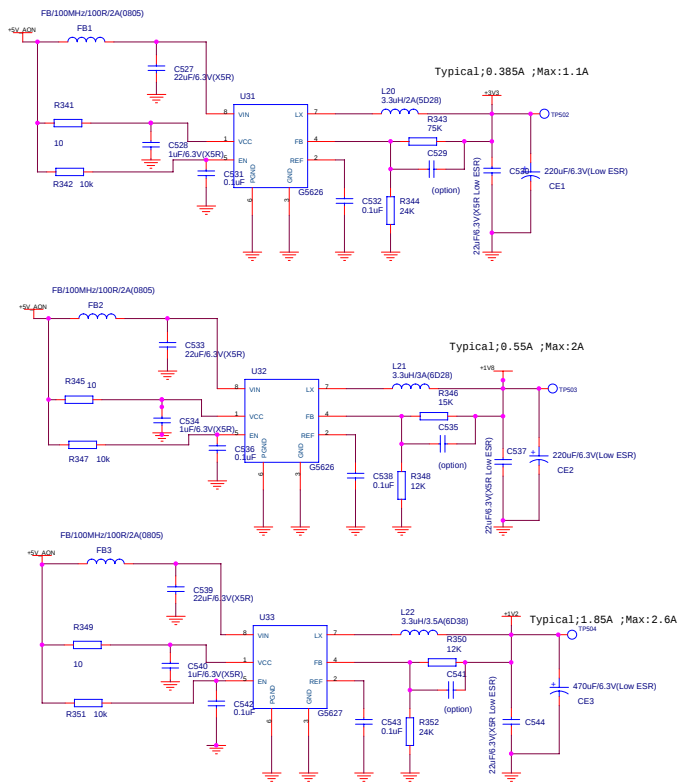
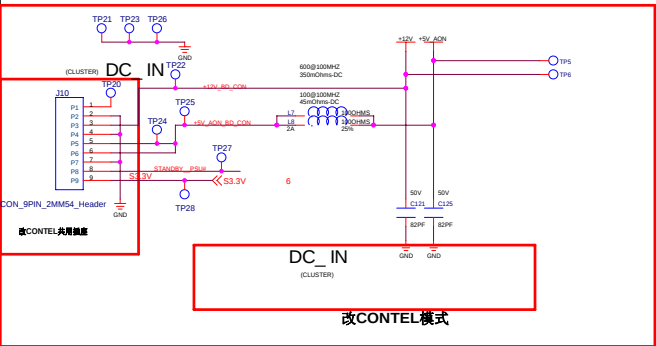


Universal CFE version requires custom DDR2 boot strap configuration.

Core Power

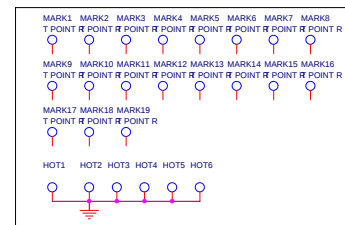
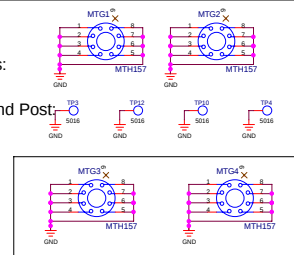


DC/DC

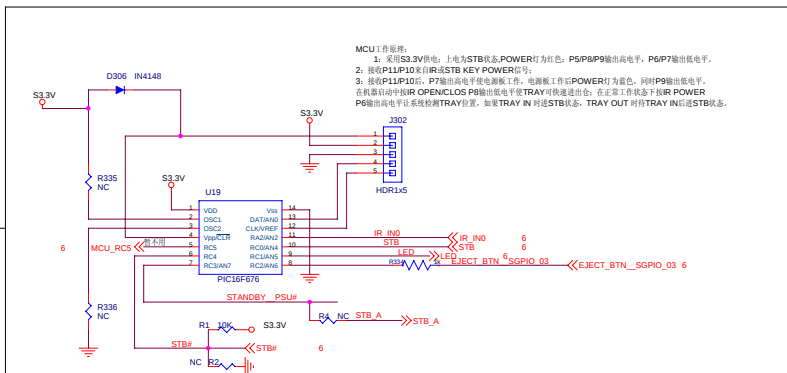


PCB Mounting Holes:

PCB Debug Ground Post:



MCU		
	add	delete
VBR 220W (not used MCU)	R4	U19 D306 R336 R336 R1 R2 R334 J302
BD200MH		R4



DC/DC Power --> Design notes and Layout Guidelines:

- 1- Note that any current consumption given for each rail are estimated. They must be measured with the complete player application running.
- 2- Power sequencing: 3.3V, 1.8V and 1.2V ramp up at the same time.

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